1 Register Address Map

Figure 1 shows the address map for the major blocks within Astro's 256KB of configuration space. Individual register addresses will be expressed as offsets within one of the ranges.

The lower half of the address space is used for registers that resides in the Runway frequency domain. Transactions with addresses in this range (0xFF_FED0_0000 to 0xFF_FED1_FFFF)

0xFF_FED3_FFFF 0xFF_FED3_E000	Rope7	8KB
0x_FF_FED3_DFFF 0xFF_FED3_C000	Rope6	8KB
0xFF_FED3_BFFF 0xFF_FED3_A000	Rope5	8KB
0xFF_FED3_9FFF 0xFF_FED3_8000	Rope4	8KB
0xFF_FED3_7FFF 0xFF_FED3_6000	Rope3	8KB
0xFF_FED3_5FFF 0xFF_FED3_4000	Rope2	8KB
0xFF_FED3_3FFF 0xFF_FED3_2000	Rope1	8KB
0xFF_FED3_1FFF 0xFF_FED3_0000	Rope0	8KB
0xFF_FED2_FFFF 0xFF_FED2_0000	IOC (133MHz)	64KB
0xFF_FED1_FFFF 0xFF_FED1_8000	Performance Counters	32KB
0xFF_FED1_7FFF 0xFF_FED1_0000	Memory Controller	32KB
0xFF_FED0_FFFF 0xFF_FED0_8000	Runway I/F	32KB
0xFF_FED0_7FFF 0xFF_FED0_0000	IOC (125MHZ)	32KB

Figure 1: Astro Register Address Map

will end up on the R2I_regbus with target registers located in the IOC, RBIB, MC or performance counters. The upper half of the address space is used for registers that reside in the I/O frequency domain. These transactions will be forwarded to the Command data fifo (in the aioc) and synchronized across the frequency domain boundary. Bit 16 of the address is used to determine if the transaction should be forwarded to a rope or destined for a register within the iioc block. If the register is located in a rope device, then bits 15:13 of the address will be used to specify the rope number of the destination.

1.1 Memory Controller Registers

Registers in the memory controller block are the target for all transactions in the range 0xFF_FED1_0000 - 0xFF_FED1_7FFF. Table 1 lists all registers in this block with their relative offset and brief description. A detailed description of the register can be found on the page listed in the cross-ref field.

Offset	Name	Description	Cross Ref
0x0200	MEM_CONTROL_0	Timing values and mode control for the DRAM control logic	
0x0208	MEM_CONTROL_1	Timing values and mode control for the DRAM control logic	
0x0210	REFRESH_INTERVAL	Control for frequency of DRAM refreshes, and other refresh related parameters	
0x0400	MBAT_ADDR_0[0]	Lower half of MBAT 0 configuration register	
0x0408	MBAT_ADDR_1[0]	Upper half of MBAT 0 configuration register	
0x0410	MBAT_ADDR_0[1]	Lower half of MBAT 1 configuration register	
0x0418	MBAT_ADDR_1[1]	Upper half of MBAT 1 configuration register	
0x0420	MBAT_ADDR_0[2]	Lower half of MBAT 2 configuration register	
0x0428	MBAT_ADDR_1[2]	Upper half of MBAT 2 configuration register	
0x0430	MBAT_ADDR_0[3]	Lower half of MBAT 3 configuration register	

Offset	Name	Description	Cross Ref
0x0438	MBAT_ADDR_1[3]	Upper half of MBAT 3 configuration register	
0x0440	MBAT_ADDR_0[4]	Lower half of MBAT 4 configuration register	
0x0448	MBAT_ADDR_1[4]	Upper half of MBAT 4 configuration register	
0x0450	MBAT_ADDR_0[5]	Lower half of MBAT 5 configuration register	
0x0458	MBAT_ADDR_1[5]	Upper half of MBAT 5 configuration register	
0x0460	MBAT_ADDR_0[6]	Lower half of MBAT 6 configuration register	
0x0468	MBAT_ADDR_1[6]	Upper half of MBAT 6 configuration register	
0x0470	MBAT_ADDR_0[7]	Lower half of MBAT 7 configuration register	
0x0478	MBAT_ADDR_1[7]	Upper half of MBAT 7 configuration register	
0x1440	MEM_SYND	Syndrome for an uncorrectable memory error	
0x1448	MEM_SYND_CORR	Syndrome for a correctable memory error	
0x1450	ECC_OVERWRITE	Check bits to directly read from and write to memory for test purposes	
0x1458	ECC_OVERWRITE_EN	Enable bit to use the ECC_OVERWRITE register	

Table 1: Memory Controller Registers

1.2 Runway Bus I/F Registers

Registers in the Runway bus I/F block are the target for all transactions in the range 0xFF_FED0_8000 - 0xFF_FED0_FFFF. Table 2 lists all registers in this block with their relative offset and brief description. A detailed description of the register can be found on the page listed in the cross-ref field.

Offset	Name	Description	Cross Ref
0x0000	MEM_SIZE	The memory size register specifies the amount of memory installed in the system.	
0x0008	MEM_HOLE_RELOC	The memory hole relocation register specifies where the 256MB I/O space memory hole is relocated.	
0x0010	ERROR_CONTROL	The error control register controls the clearing of “stat” and “over” bits in the ERROR_STATUS register and clearing of error logging registers.	
0x0018	ERROR_ENABLE	The error enable register enables the signaling and logging of errors.	
0x0020	ERROR_STATUS	The error status register indicates which, if any, errors have occurred one or more times.	
0x0038	RUN_CTRL	The Runway control register saves the state of Runway control signals when either ADDR_VALID or DATA_VALID are asserted.	
0x0040	RUN_ADDR	The Runway address register saves the state of the ADDR_DATA bus when ADDR_VALID is asserted.	
0x0048	RUN_DATA_HIGH	The Runway data high register saves the state of bits 0-63 of the ADDR_DATA bus when DATA_VALID is asserted.	
0x0050	RUN_DATA_LOW	The Runway data low register saves the state of bits 64-127 of the ADDR_DATA bus when DATA_VALID is asserted.	

Offset	Name	Description	Cross Ref
0x4000	RBIB_CTRL	The Runway bus interface block control register configures Runway flow control and coherency map features.	
0x4008	MEM_ADDR	The memory address register stores the master ID, transaction ID, and memory address of an uncorrectable memory error.	
0x4010	MEM_ADDR_CORR	The memory address correctable register stores the master ID, transaction ID, and memory address of a correctable memory error.	
0x4100 to 0x4178	WCM_DIAG_READ[0:15]	The write coherency map diagnostic read register allows diagnostic code to read the state of the write coherency map.	
0x4180 to 0x41F8	RCM_DIAG_READ[0:15]	The read coherency map diagnostic read register allows diagnostic code to read the state of the read coherency map.	

Table 2: Runway I/F Registers

1.3 R2I Registers

The R2I block is the target for all transactions in the range 0xFF_FED0_0000 - 0xFF_FED0_7FFF.

Offset	Name	Description	Cross Ref
0x0000	ID	Astro Identification register	
0x0008	IOC_CTRL	IOC control register	
0x0010	TOC _CLIENT_ID	TOC Monarch client ID register - used to select which CPU will receive TOCs	
0x0300	LMMIO_DIRECT0_BASE	Sets the starting address for direct range0.	
0x0308	LMMIO_DIRECT0_MASK	Sets the size of direct range0	
0x0310	LMMIO_DIRECT0_ROUTE	Specifies the rope number for direct range0	

Offset	Name	Description	Cross Ref
0x0318	LMMIO_DIRECT1_BASE	Sets the starting address for direct range1.	
0x0320	LMMIO_DIRECT1_MASK	Sets the size of direct range1	
0x0328	LMMIO_DIRECT1_ROUTE	Specifies the rope number for direct range1	
0x0330	LMMIO_DIRECT2_BASE	Sets the starting address for direct range2.	
0x0338	LMMIO_DIRECT2_MASK	Sets the size of direct range2	
0x0340	LMMIO_DIRECT2_ROUTE	Specifies the rope number for direct range2	
0x0348	LMMIO_DIRECT3_BASE	Sets the starting address for direct range3.	
0x0350	LMMIO_DIRECT3_MASK	Sets the size of direct range3	
0x0358	LMMIO_DIRECT3_ROUTE	Specifies the rope number for direct range3	
0x0360	LMMIO_DIST_BASE	Sets the starting address for the LMMIO distributed range.	
0x0368	LMMIO_DIST_MASK	Sets the size of the LMMIO distributed range.	
0x0370	LMMIO_DIST_ROUTE	Specifies the address bit that corresponds to the least significant bit of the rope number when in the LMMIO range.	
0x0378	GMMIO_DIST_BASE	Sets the starting address for the GMMIO distributed range.	
0x0380	GMMIO_DIST_MASK	Sets the size of the GMMIO distributed range.	
0x0388	GMMIO_DIST_ROUTE	Specifies the address bit that corresponds to the least significant bit of the rope number when in the GMMIO range.	
0x0390	IOS_DIST_BASE	Sets the starting address for the GMMIO distributed range.	
0x0308	IOS_DIST_MASK	Sets the size of the GMMIO distributed range.	
0x03A0	IOS_DIST_ROUTE	Specifies the address bit that corresponds to the least significant bit of the rope	

Offset	Name	Description	Cross Ref
		number when in the IOS distributed range.	
0x03C0	IOS_DIRECT_BASE	Sets the starting address for the direct IOS range.	
0x03C8	IOS_DIRECT_MASK	Sets the size of the direct IOS range.	
0x03D0	IOS_DIRECT_ROUTE	Specifies the rope number for direct range.	
0x4200	GRFC0	Graphics flow control register 0	
0x5200	GRFC1	Graphics flow control register 1	
0x6200	GRFC2	Graphics flow control register 2	
0x7200	GRFC3	Graphics flow control register 3	

Table 3: R2I Registers

1.4 IIOC Registers

Transactions with addresses from 0xFF_FED2_0000 to 0xFF_FED2_FFFF will be forwarded to the IIOC block.

Offset	Register
0x2000	FUNC_ID
0x2008	FUNC_CLASS
0x2040	Rope Config
0x2050	Rope_debug
0x2108	STATUS_CONTROL
0x2200	Rope0_Control
0x2208	Rope1_Control
0x2210	Rope2_Control
0x2218	Rope3_Control
0x2220	Rope4_Control
0x2228	Rope5_Control
0x2230	Rope6_Control
0x2238	Rope7_Control

Offset	Register
0x2300	TLB_IBASE
0x2308	TLB_IMASK
0x2310	TLB_PCOM
0x2318	TLB_TCNFG
0x2320	TLB_PDIR_BASE
0x2340	DIAG_WRT
0x2348	DIAG_RD
0x2350	DIAG_CMD
0x2358	AGP_min_per_gnt
0x2400	FLUSH_CTRL
0x2408	CTAG_CMP
0x2480	CTAG0
0x2488	CTAG1
0x2490	CTAG2
|	|
0x24FF	CTAG15
0x2680	Rope0_Err_Code
0x2688	Rope1_Err_Code
0x2690	Rope2_Err_Code
0x2698	Rope3_Err_Code
0x26A0	Rope4_Err_Code
0x26A8	Rope5_Err_Code
0x26B0	Rope6_Err_Code
0x26B8	Rope7_Err_Code
0x26C0	Rope_timeout
0x2708	Performance Counter Configuration Register
0x2718	Mask/En 1
0x2730	Mask/En 2

Table 4: IIOC Registers

1.5 Elroy Registers

Transactions with addresses from 0xFF_FED3_0000 to 0xFF_FED3_FFFF will be forwarded to an Elroy on one of the eight ropes. Each Elroy chip has 8KB of address space for configuration. Half of this space is dedicated to the performance counters so they can live on their own page and be safely accessed by user level code. The other half contains all the other registers. Table 5 shows to offset for each function for each of eight possible Elroy's. A PIO read to a register in an Elroy that does not exist will time-out in the CPU resulting in an HPMC. Data from writes to non-existent Elroy's will be discarded. See the Elroy ERSs for the definition of specific registers within each function.

Offset	Name	Description
0x0000	Elroy0 function0	Configuration
0x1000	Elroy0 function1	Performance counters
0x2000	Elroy1 function0	Configuration
0x3000	Elroy1function1	Performance counters
0x4000	Elroy2 function0	Configuration
0x5000	Elroy2function1	Performance counters
0x6000	Elroy3 function0	Configuration
0x7000	Elroy3function1	Performance counters
0x8000	Elroy4 function0	Configuration
0x9000	Elroy4 function1	Performance counters
0xA000	Elroy5 function0	Configuration
0xB000	Elroy5 function1	Performance counters
0xC000	Elroy6 function0	Configuration
0xD000	Elroy6function1	Performance counters
0xE000	Elroy7 function0	Configuration
0xF000	Elroy7function1	Performance counters

Table 5: Elroy Function Offsets

1.6 Processor Clock Domain Performance Counter Registers

Registers in the Processor Clock Domain Performance Counter block are the target for all transactions in the range 0xFF_FED1_8000 - 0xFF_FED1_FFFF. Table 2 lists all registers in this block with their relative offset and brief description. A detailed description of the register can be found on the page listed in the cross-ref field.

Offset	Name	Description	Cross Ref
0x0000	PC_CC_CTRL_0	The control counter control register 0 controls the control performance counter.	
0x0008	PC_CC_CTRL_1	The control counter control register 1 controls the control performance counter.	
0x0020 to 0x0038	PC_EC_CTRL_0 to PC_EC_CTRL_3	The event counter control registers control each of the four event performance counters.	
0x0060	PC_HEAP_WAIT_SEL	The heap wait select register selects which types of waiting heap entries to tally into event performance counter 0.	
0x0070	PC_ADDR_MASK_0	The Runway address mask 0 register masks Runway address bits for PC_CC_CTRL_0.	
0x0078	PC_ADDR_MASK_1	The Runway address mask 1 register masks Runway address bits for PC_CC_CTRL_1.	
0x4010	PC_CC	The control counter register contains the value of the control performance counter.	
0x4040 to 0x4058	PC_EC_0 to PC_EC_3	The event counter registers contain the value of the four event performance counters.	

Table 6: Performance Counter Registers