1 System Address Map

The Astro system address map is shown in Figure 1. The address map is shown in terms of the 40-bit address as viewed from the runway bus. The same map applies whether the CPUs are running in 32-bit mode or 64-bit mode. Several areas of the address map are only accessible when running in 64-bit mode (marked OS64). The terms LMMIO, GMMIO, and I/O Port space are borrowed from Tahoe. In the Astro context, LMMIO refers to PCI transactions that have an address less than 4GB (32-bits) and can therefore be issued using a single address cycle (SAC). GMMIO refers to PCI transactions with addresses greater than 4GB and therefore require dual address cycles (DAC) to issue. I/O port space refers to PCI transactions in the I/O space (ie. they use I/O read or I/O write commands). The PCI I/O space is 64KB (16-bits of address).

1.1 32 Bit Addressing on 40 Bit Runway

Runway is a 40 bit bus, and all modules are supposed to generate and respond to 40 bit addresses. If the module has only 32 bit addresses internally, these need to be extended for use on Runway.

For addresses in the 32 bit memory address range, 0x0000_0000 to 0xEFFF_FFFF, the address is zero extended to create the 40 bit address, in the range 0x00_0000_0000 to 0x00_EFFF_FFFF. For addresses in the 32 bit I/O address range, 0xF100_0000 to 0xFFFF_FFFF, the address is “f” extended to create the 40 bit I/O addresses in the range 0xFF_F100_0000 to 0xFF_FFFF_FFFF.

PDC address space is a special case. In 40 bit physical address machines PDC is allocated the address range from 0xEF_0000_0000 to 0xEF_FFFF_FFFF for memory accesses and from 0xF0_0000_0000 to 0xF0_FFFF_FFFF for I/O space accesses. Current processors only use the PDC I/O space so will map the 32 bit PDC I/O space, 0xF000_0000 to 0xF0FF_FFFF, to the 40 bit address range, 0xF0_F000_0000 to 0xF0_F0FF_FFFF.

Astro will “F” extend peer-to-peer addresses that are generated by 32-bit PCI devices prior to driving these addresses onto Runway.

1.2 PCI LMMIO Space

This space is used to initiate PCI transactions with single cycle addresses (32-bits). The lower 32-bits of the Runway address are used for the PCI address.

This space is divided up between the 8 ropes with one distributed range and 4 directed ranges. The distributed range is divided up between the 8 ropes in equal segments. The directed ranges can be used for any single rope. Each Elroy is limited to a maximum of 2 different ranges (typically one distributed range an one directed range would be the maximum used for a single Elroy). All ranges start at any naturally aligned location within the LMMIO space and must be a power of 2 in size. See the IOC chapter for details.

0xFF_FFFF_FFFF 0xFF_FFFC_0000	broadcast space	256KB
0xFF_FFFB_FFFF 0xFF_FFF8_0000	Runway HPA space	256KB
0xFF_FFF7_FFFF 0xFF_FF00_0000	unused	16MB- 512K
0xFF_FEFF_FFFF 0xFF_FEF0_0000	Interrupt Acknowledge	1MB
0xFF_FEEF_FFFF 0xFF_FEE8_0000	unused	512KB
0xFF_FEE7_FFFF 0xFF_FEE0_0000	PCI I/O Port Space	512KB
0xFF_FEDF_FFFF 0xFF_FED4_0000	unused	768KB
0xFF_FED3_FFFF 0xFF_FED0_0000	Astro Configuration	256KB
0xFF_FECF_FFFF 0xFF_F100_0000	PCI LMMIO	221MB
0xFF_F0FF_FFFF 0xFF_0000_0000	unused	4GB - 240MB
0xFE_FFFF_FFFF 0xF1_0000_0000	PCI GMMIO (64)	56GB
0xF0_FFFF_FFFF 0xF0_F100_0000	unused	240MB
0xF0_F0FF_FFFF 0xF0_F000_0000	PDC space	16MB
0xF0_EFFF_FFFF 0xF0_0000_0000	unused PDC space	4GB - 256MB
0xEF_FFFF_FFFF 0xEF_0000_0000	cacheable PDC space	4GB
0xEE_FFFF_FFFF 0x11_0000_0000	unused	888GB
0x10_FFFF_FFFF 0x10_F000_0000	main memory space1 (64)	256MB
0x10_EFFF_FFFF 0x10_0000_0000	unused	4GB- 256MB
0x0F_FFFF_FFFF 0x01_0000_0000	main memory space2 (64)	60GB
0x00_FFFF_FFFF 0x00_F000_0000	unused	256MB
0x00_EFFF_FFFF 0x00_0000_0000	main memory space0	4GB- 256MB

I/O Space

Memory Space

Figure 1: Astro System Address Map

1.3 PCI I/O Port Space (IOP)

Write_short or read_short transactions to either of the two PCI I/O port spaces are used to initiate a PCI I/O Port space transaction on PCI. Only one of the two available ranges would be used at any given time. All IOP writes will be posted.

The IOP range from 0xFF_FEE0_0000 to 0xFF_FEEF_FFFF is used when CPUs are running in a 32-bit mode. This range contains one distributed range and one directed range. The distributed range can be expanded all the way up to 512KB which allows direct access to all IOP locations on all ropes. Inter-rope P2P will not work if this range is made larger the 64KB and is therefore strongly discouraged. The directed range is provided to support busses that need a large amount of IOP space (such as expander boxes).

The I/O port space range from 0xF8_0000_0000 to 0xF8_03FF_FFFF is available when running with a 64-bit OS. It is contains a single distributed range.

1.4 PCI GMMIO Space

This space is used to initiate PCI transactions with dual cycle addresses (64-bits). All 40-bits of the Runway address are used for the PCI address.

The GMMIO space is only accessible when the CPU is running in 64-bit mode. It contains a single distributed range with a fixed base and size.

1.5 PDC I/O Space

Astro's PDC address range goes from 0xF0_F000_0000 to 0xF0_F0FF_FFFF. This space in used for the boot ROMs and PDH. Astro will detect the presence of Dillon be sampling the sense of the "ready" signal on the PDH bus at the end of reset. If Dillon is present, transactions in this range will be forwarded to Dillon. If Dillon is not present, addresses in this range will forwarded to rope0. PDC addresses which are forwarded to rope0 (rope0_adr[31:0]) will be calculated from the Runway address (rw_adr) using the following algorithm.

```
rope0_adr[15:0]=rw_adr[15:0];
rope0_adr[31:24]=8'h00;
 If (rw_adr[23:16]==8'h00) rope0_adr[23:16]=8'h0F;
else rop0_adr[23:16]=rw_adr[23:16];
```

1.6 Memory Space

Main memory can live in 3 different locations in the address map as shown in Figure 1. Memory always starts at location 0x00_0000_0000 in memory space0. It is added in a contiguous fashion until space0 is full and then jumps to location 0x10_F000_0000 in space1. When space0 and space1 are full, memory is added at location 0x01_0000_0000 in space2. Note that only space0 is accessible when the CPU is running in 32-bit mode. The memory hole from 0x00_F000_0000 to 0x00_FFFF_FFFF is necessary to allow rope-to-rope peer-to-peer transactions with 32-bit PCI devices. Elroy will recognize this space as I/O space and do an I/O transaction. Astro will "F"-extend the address before it reaches Runway so addresses in this range will never be seen on Runway. If memory was allowed in this space it would not be available for DMA by devices that do not use the TLB (Note: The only devices that are not required to use the TLB for DMA are ones that encode the virtual index into the upper bits of their address).

1.7 Astro Configuration Space

The Astro configuration space (not to be confused with PCI configuration space) is used to access registers in Astro. Elroy is treated as part of Astro from a programming model point of view. Their registers are therefore accessed via the Astro configuration space as well. All Astro registers are assigned to fixed addresses. The Astro configuration space is divided into two halves. One half of the addresses are used for registers in the Runway frequency domain (125MHz) and the other half are used for addresses in the IO frequency domain (133MHz). Addresses in the IO frequency domain are split equally between Elroy registers and registers actually residing on the Astro chip. Registers in the Runway frequency domain are split equally between the AIOC, the MC, the RBIB, and unused. See the Astro register map chapter for more details.

1.8 Interrupt Acknowledge

Read_short transactions to locations in the interrupt acknowledge space will result in the AIOC performing an INT_ACK transaction. The recommended location for this operation is 0xFF_FEFF_0000.

1.9 Cacheable PDC Space

Astro's PDC can be accessed through memory space as well as I/O space. The advantage of the memory space is that it uses 64-byte cacheline accesses which are more efficient with Dillon and that the CPU can store the information in it's local instruction cache. This space is restricted to non-coherent read access only.